

Abstract Of The Disclosure

A high speed voltage mode sensing is provided for a digital multibit non-volatile memory integrated system. An embodiment has a local source follower stage followed by a high speed common source stage. Another embodiment has a local source follower stage followed by a high speed source follower stage. Another embodiment has a common source stage followed by a source follower. An auto zeroing scheme is used. A capacitor sensing scheme is used. Multilevel parallel operation is described.